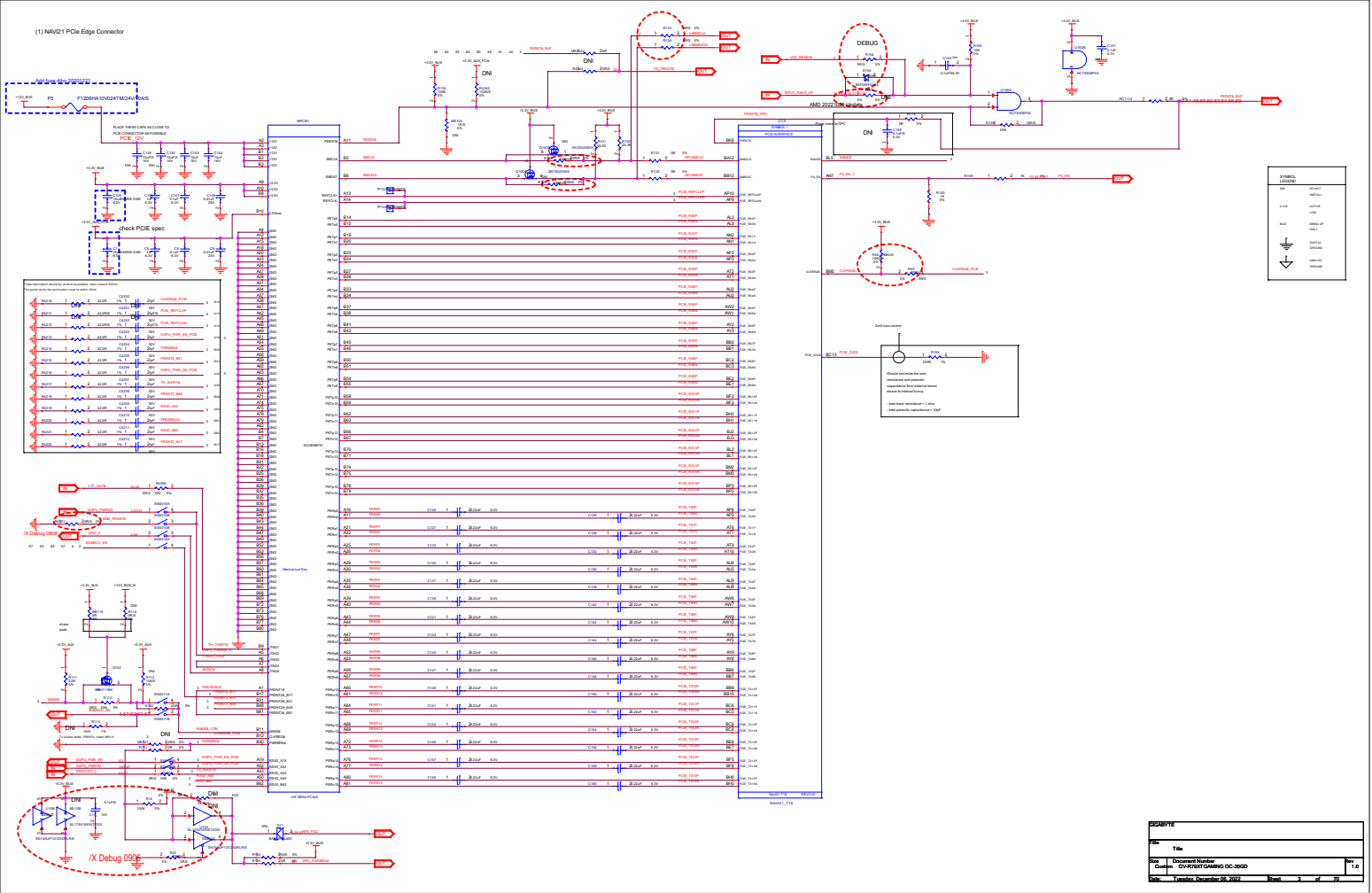


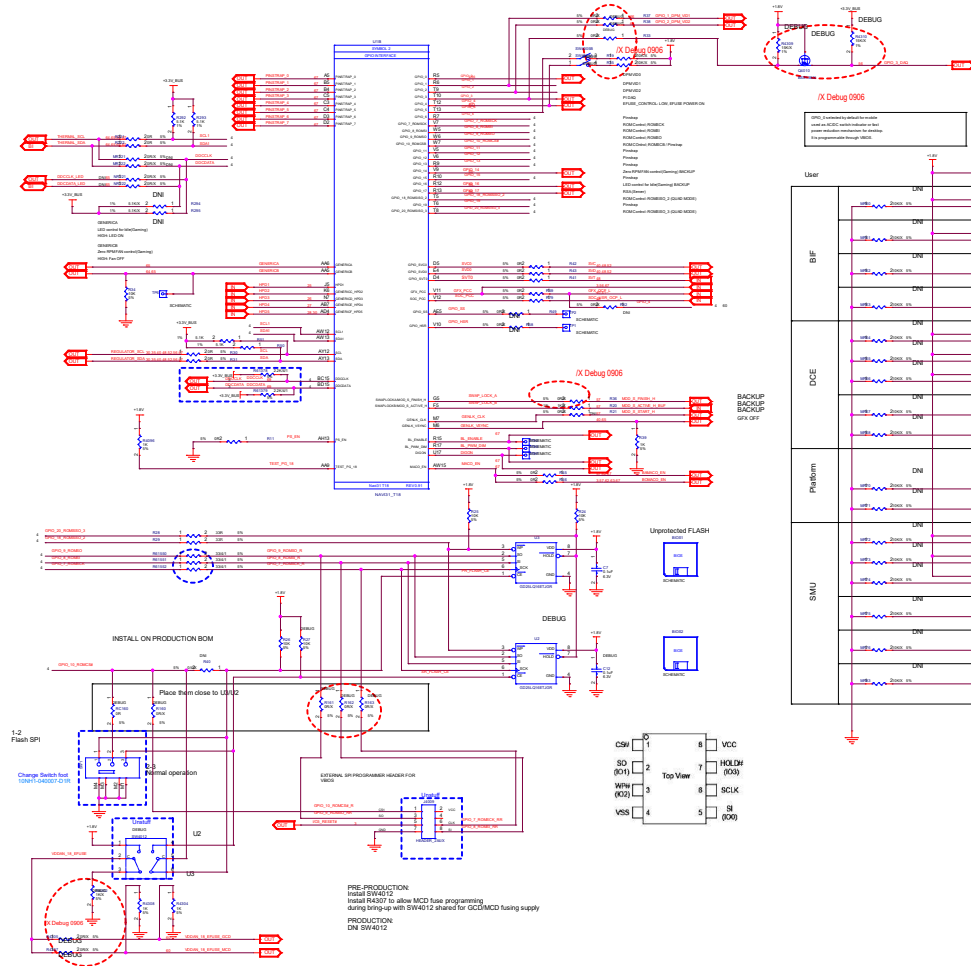
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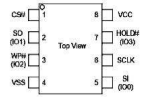


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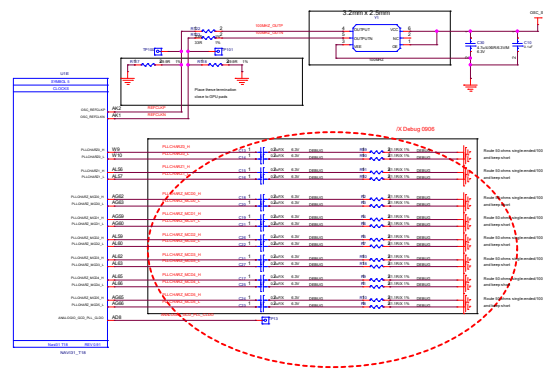
Note: Internal LUTs at GCD pad is **0000** in binary design spec

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	2	PINSTRAP_BIF_LC_TX_SWING	0	PINSTRAP_BIF_LC_TX_SWING
	3	PINSTRAP_BIF_VGA_DIS	0	PINSTRAP_BIF_VGA_DIS
DCE	4	PINSTRAP_AUD_PORT_CONN2[0]	0	PINSTRAP_AUD_PORT_CONN2[0]
	5	PINSTRAP_AUD[0]	0	PINSTRAP_AUD[0]
	6	PINSTRAP_AUD[1]	0	PINSTRAP_AUD[1]
	7	PINSTRAP_AUD[2]	0	PINSTRAP_AUD[2]
Platform	8	PINSTRAP_BOARD_CONFIG[0]	0	TBD
	9	PINSTRAP_ROM_CONFIG[0]	1	PINSTRAP_ROM_CONFIG[0]
SMU	10	PINSTRAP_SMBUS_ADDR	0	PINSTRAP_SMBUS_ADDR
	11	PINSTRAP_BIOS_ROM_EN	1	PINSTRAP_BIOS_ROM_EN
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	13			



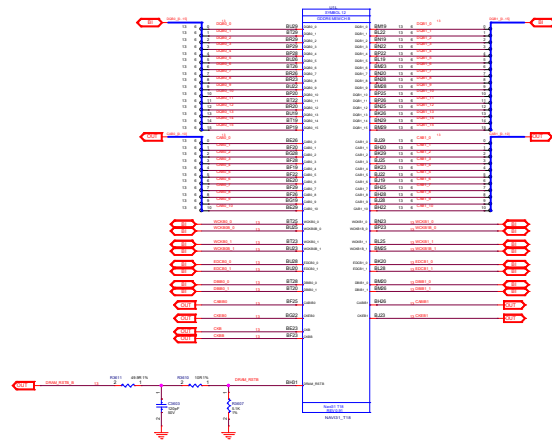
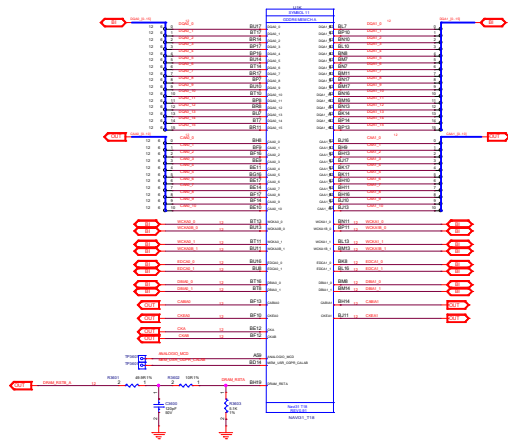
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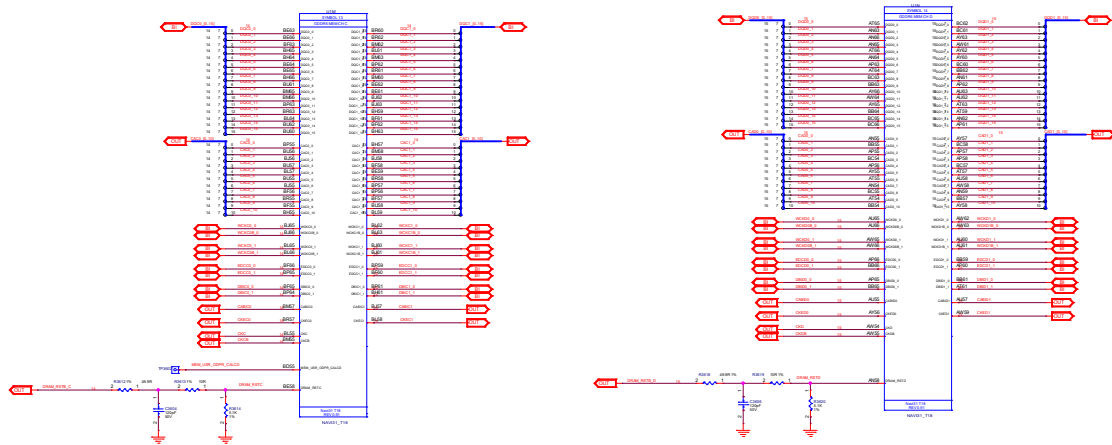


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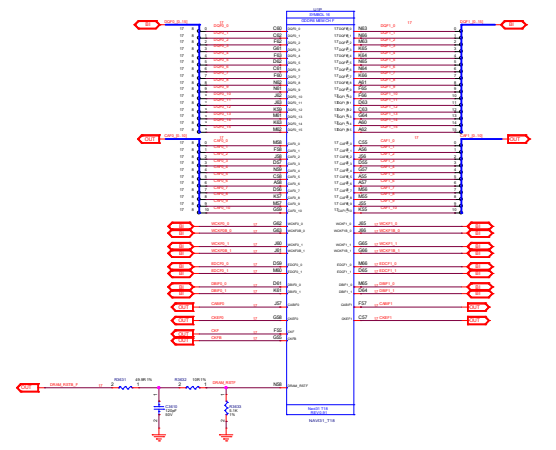
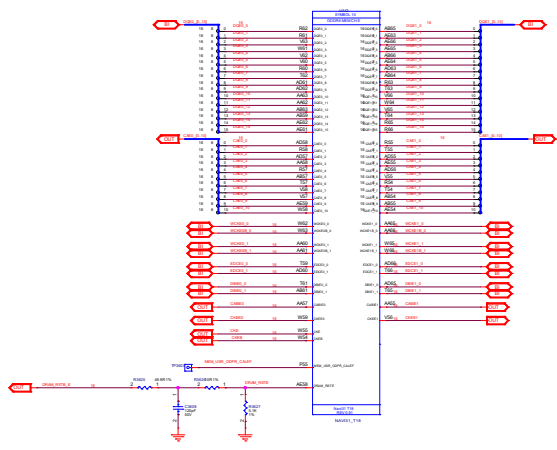


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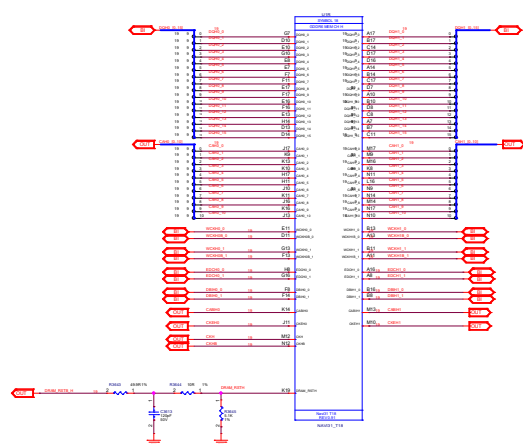
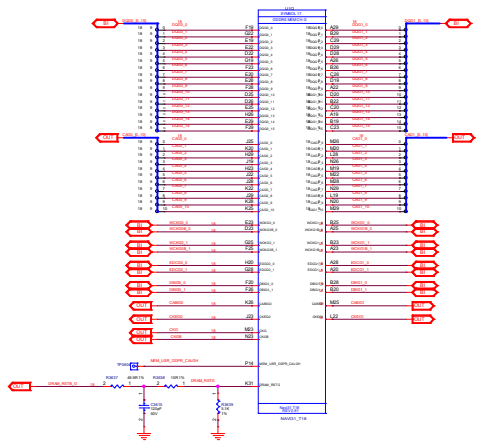
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MEM I/F is available only for calibration boards
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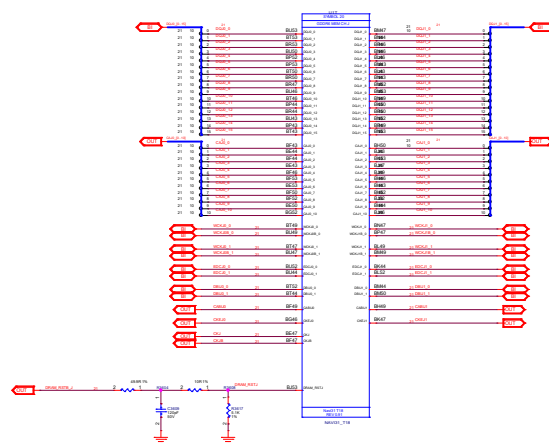
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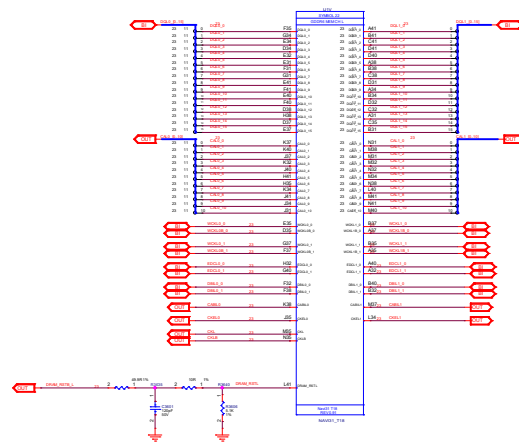
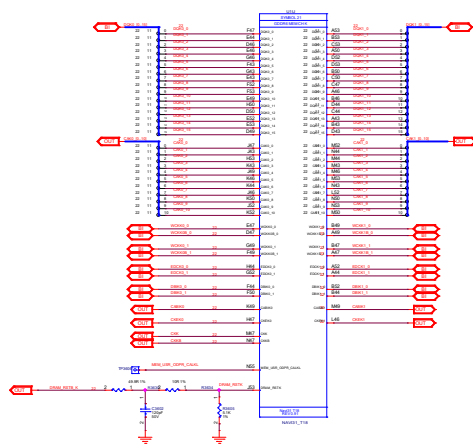


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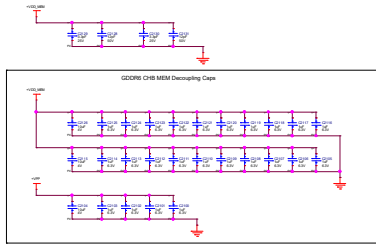


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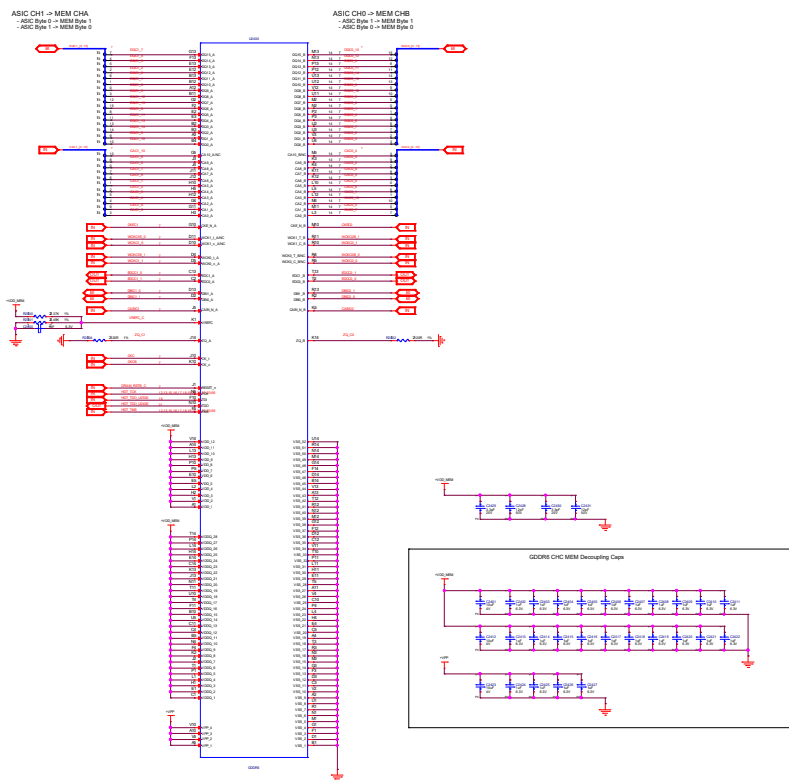


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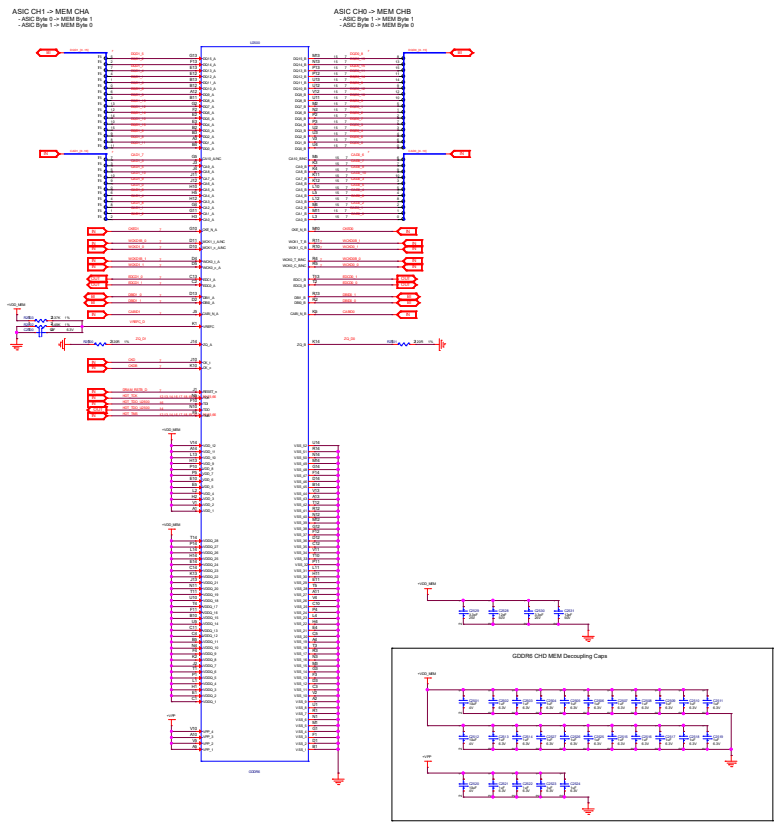
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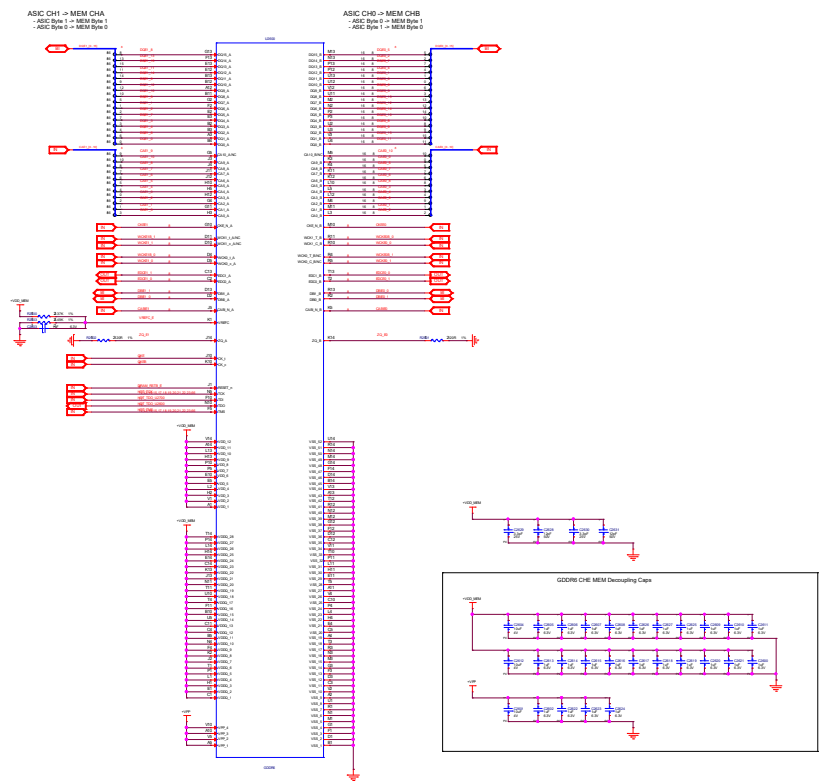
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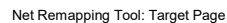
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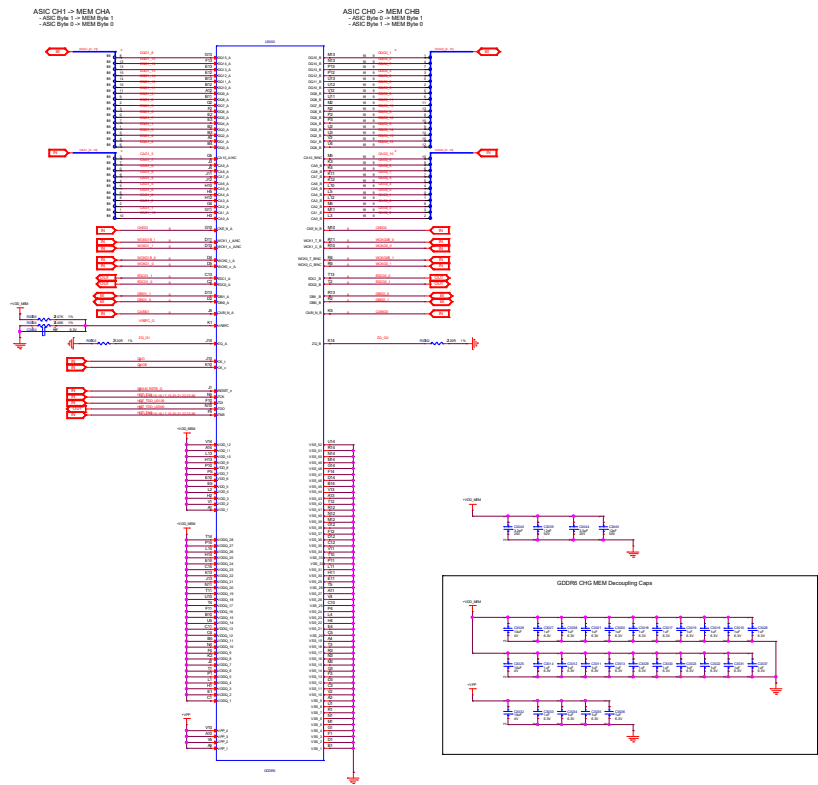
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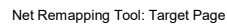


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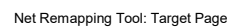


Net Remapping Tool: Target Page

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Rev	1.0
GDDR6 MEM Decoupling Caps	
Rev	1.0
Version	1.0
Author	1.0
Rev	1.0



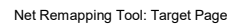
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Date:	Tuesday, December 04, 2022	Sheet	13 of 30



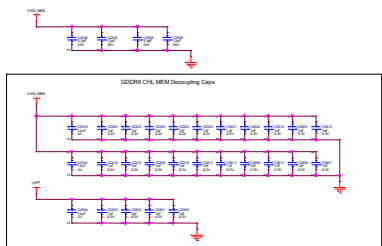
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Date:	Thursday, December 04, 2008	Sheet	20 of 70



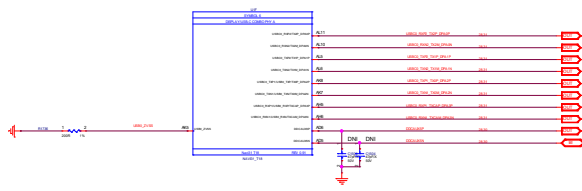
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Created: December 06, 2002		Printed: 04/06/03	



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Ver	1.0
Date	Tuesday, December 04, 2022
Sheet	32 of 36

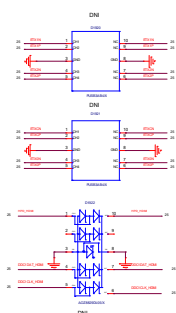
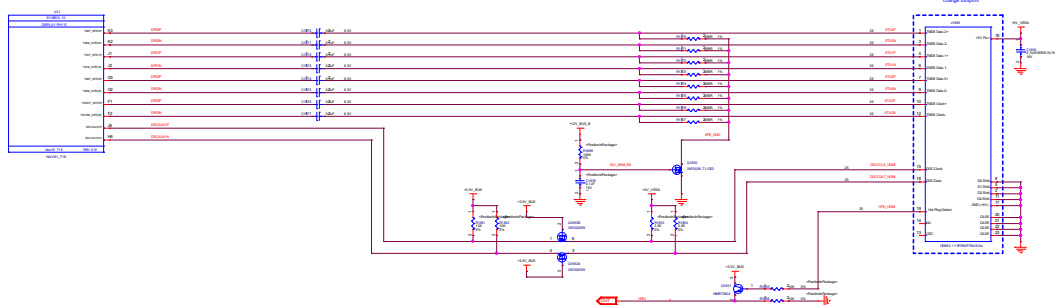


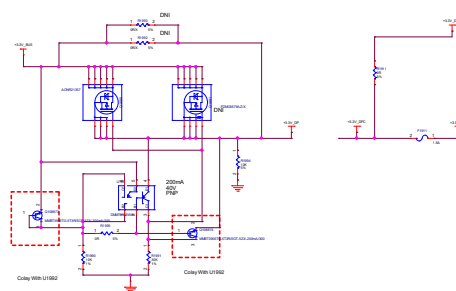
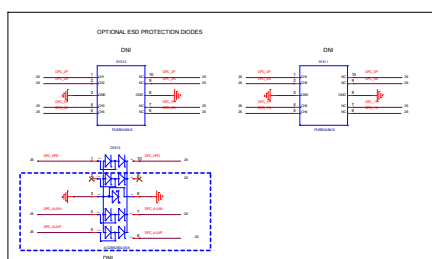
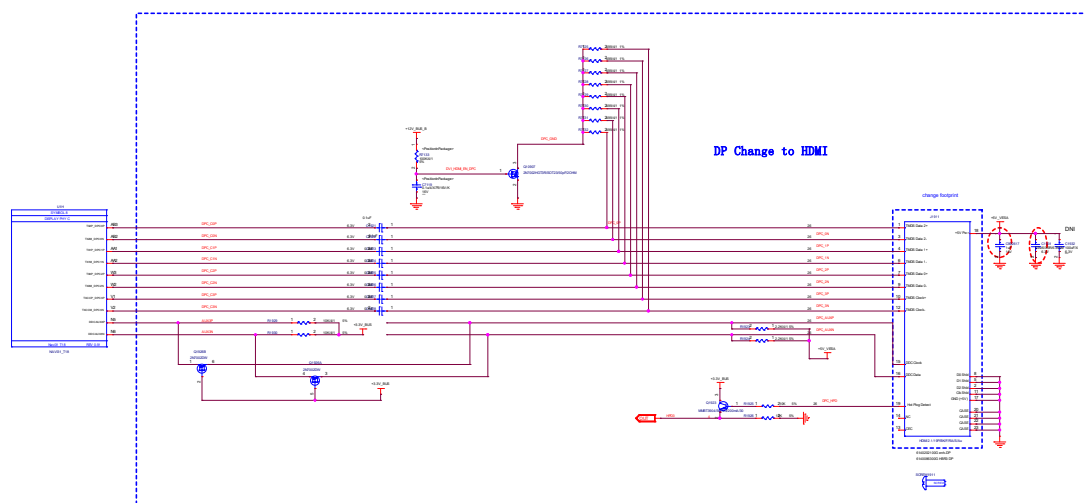
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Date:	Tuesday December 06, 2022	Event:	75	of	30

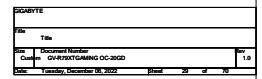


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Author	Gustavo Henrique		
Company	Gustavo Henrique CC Ltda		
Date	Monday, October 19, 2025	Sheet	24 of 24

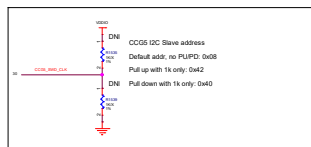




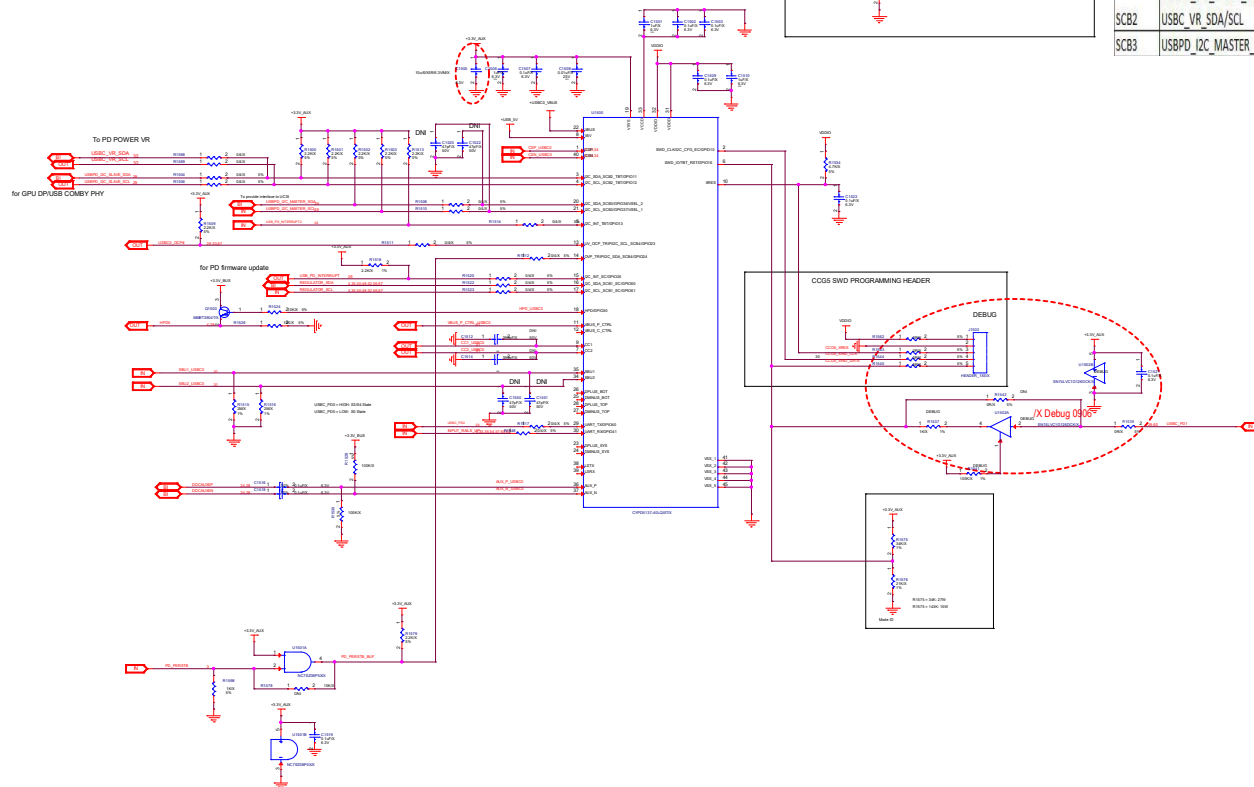


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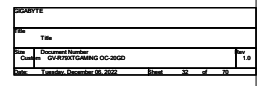


CCG5	Nav10	Note
SCB1	SDA/SCL	Firmware update/SMU
SCB2	USBPD_I2C_SLAVE_SDA/SCL	Nav10 MUX/PD_Regulator/re-driver
SCB3	USBPD_I2C_MASTER_SDA/SCL	UCSI

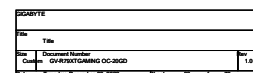


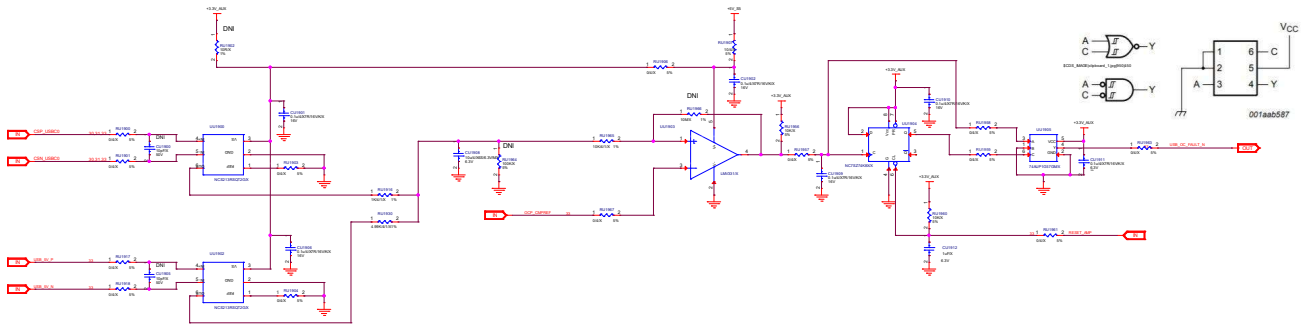
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Released	09/09/2019

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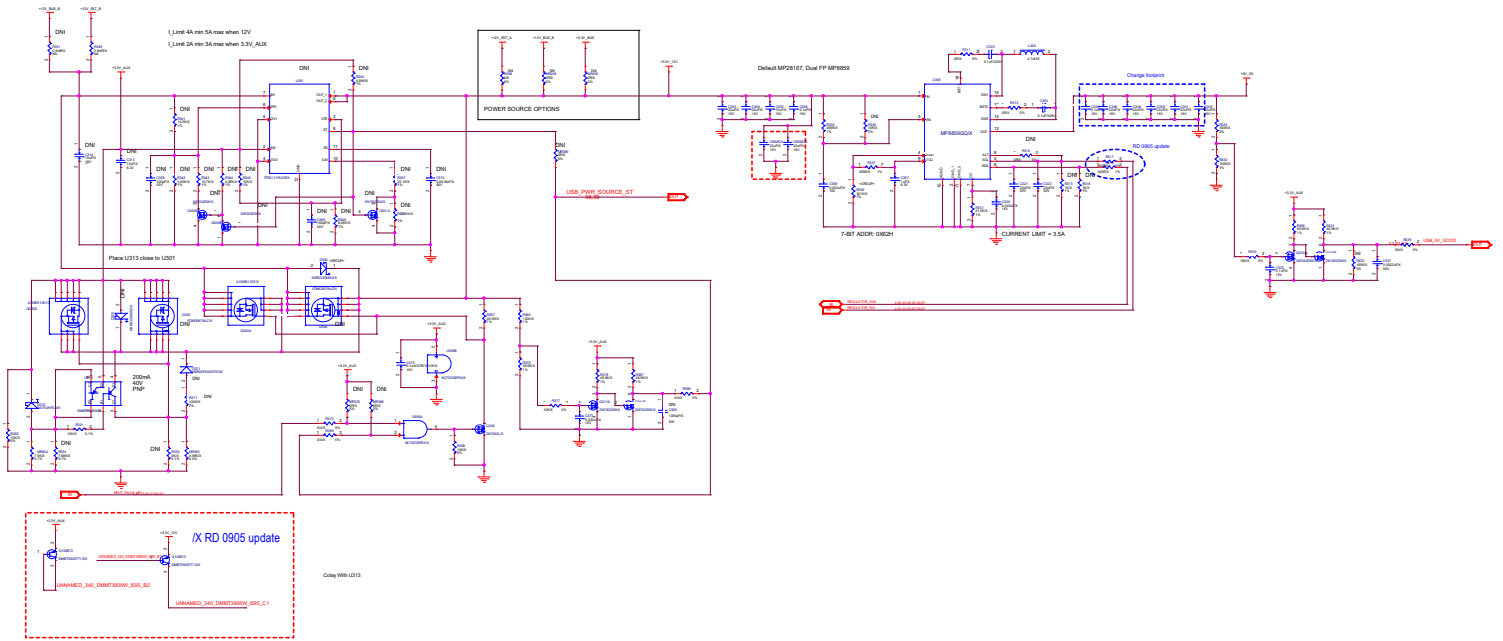
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OUTPUT MODE	RESET PIN SETTING
Transparent	RESET = low
Latch	RESET = high

GIGABYTE				
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File	Document Number			Rev
Customer	GV-R79XTGAMING OC-30GD			1.0
Date:	Tuesday, December 05, 2023		Page	34 of 35

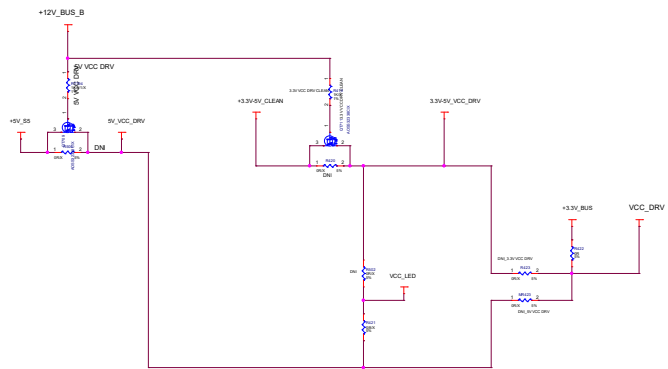


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3	3	Revise to match CC-001	01-01-2020

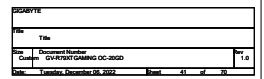


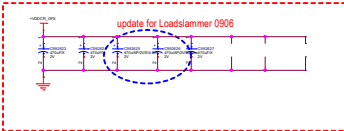
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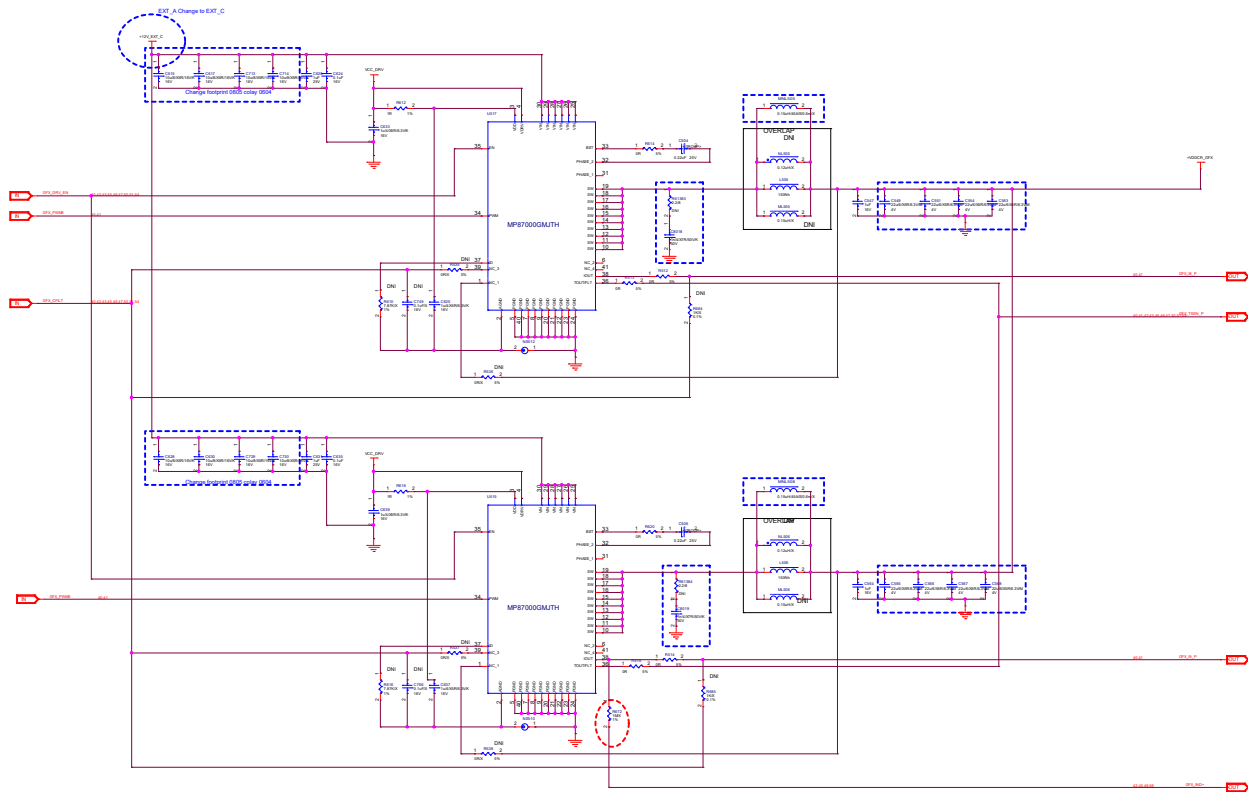
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Ver	Revision	Created	1 of 1

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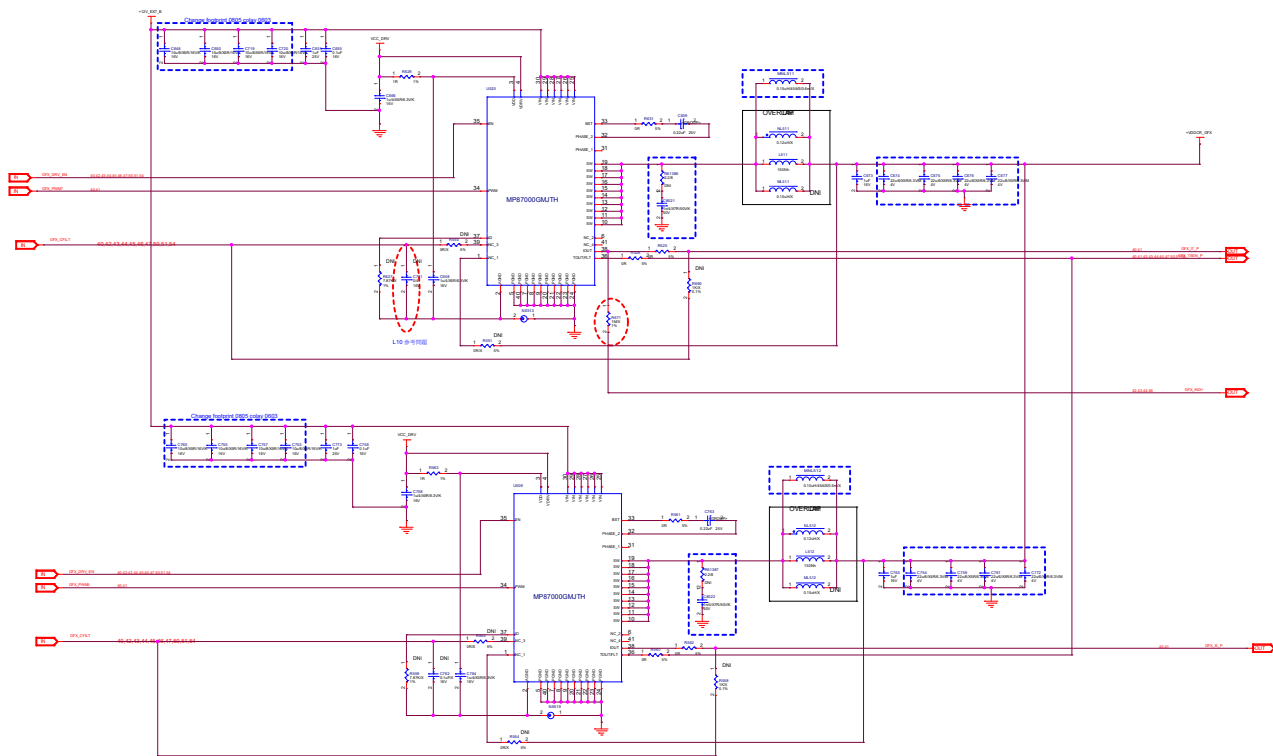


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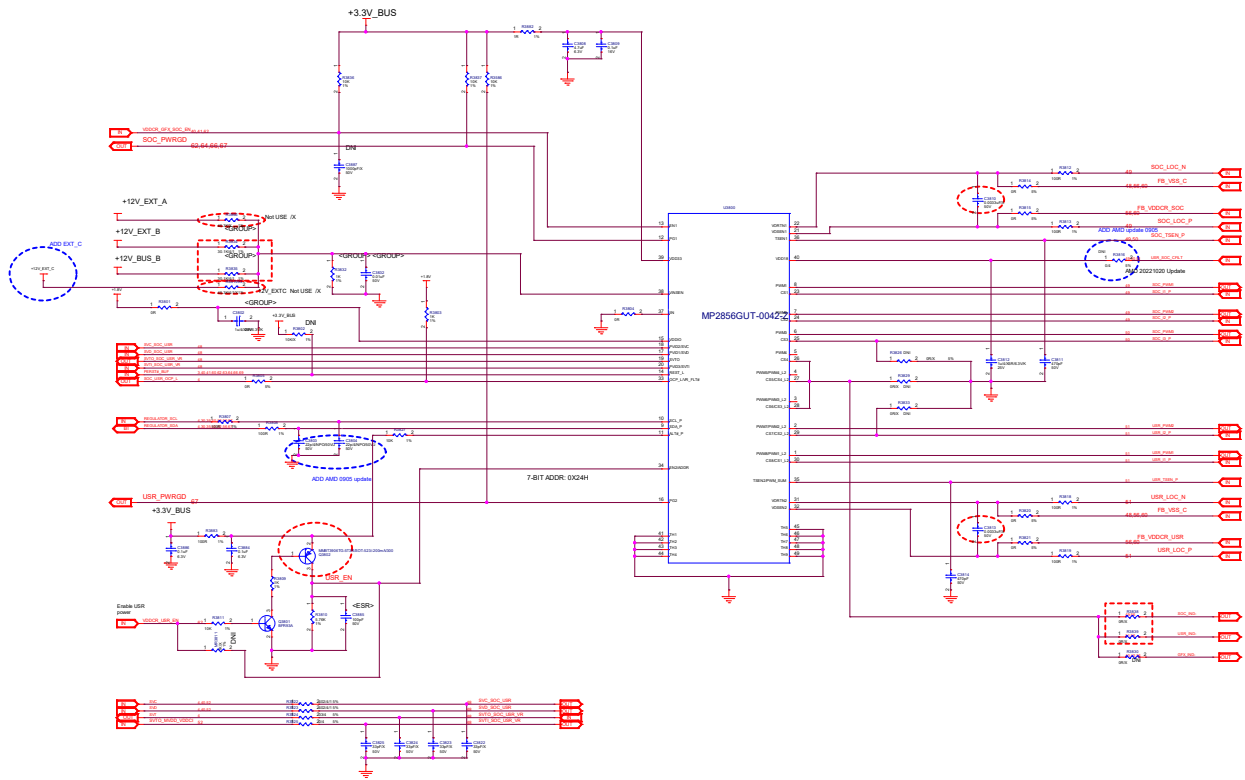
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3	1.2	Final Release	2023-10-10

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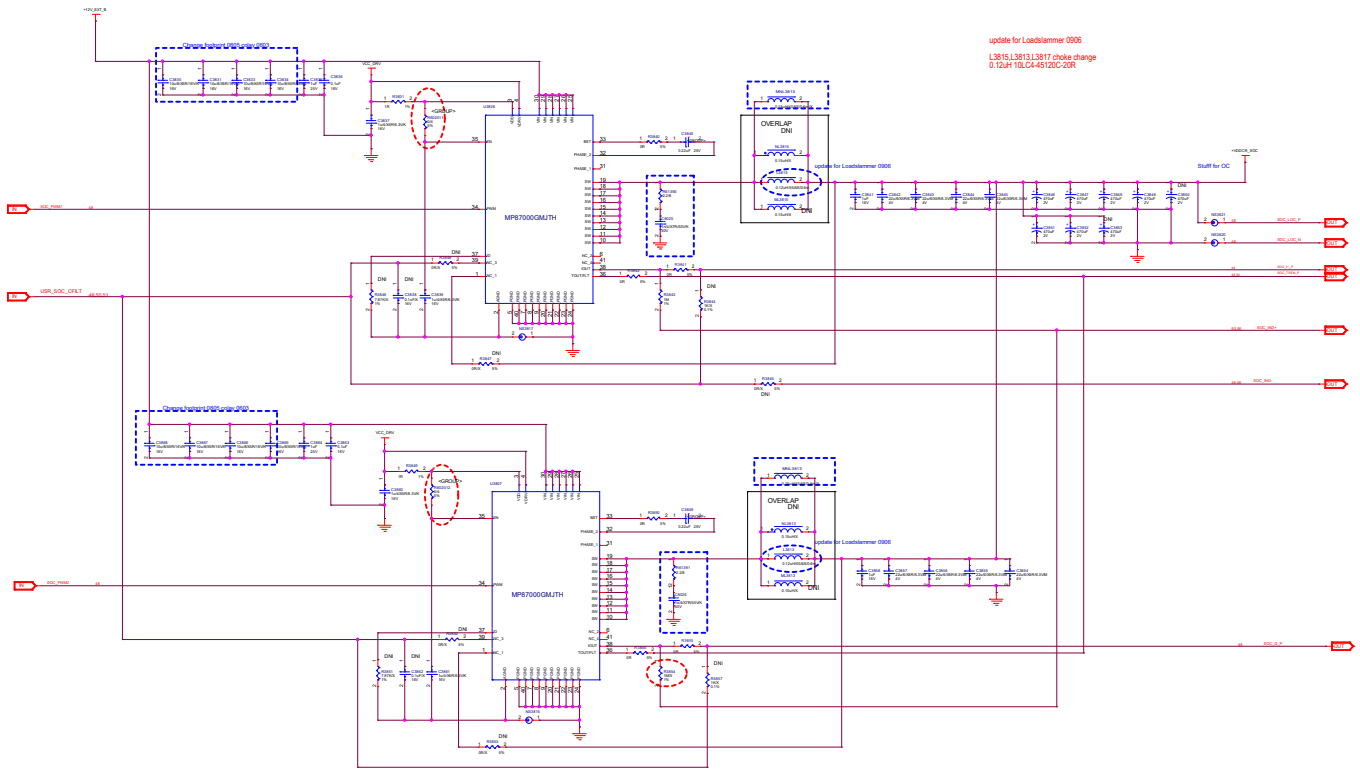


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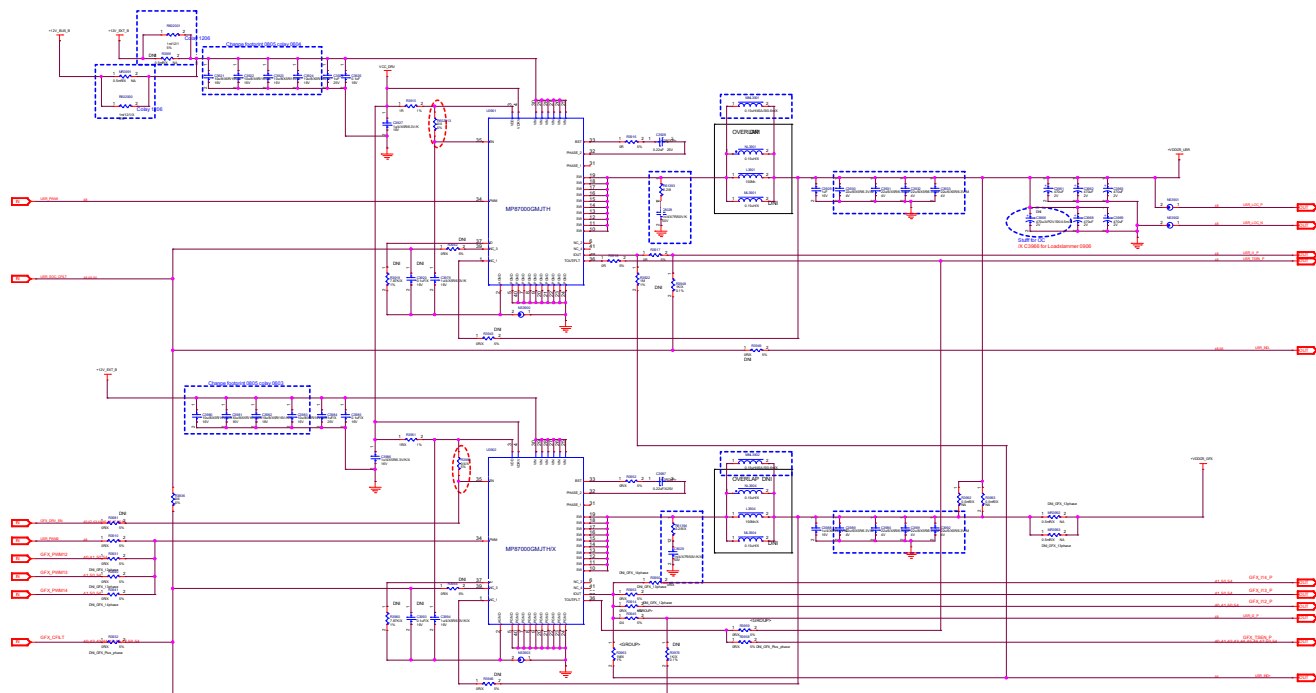


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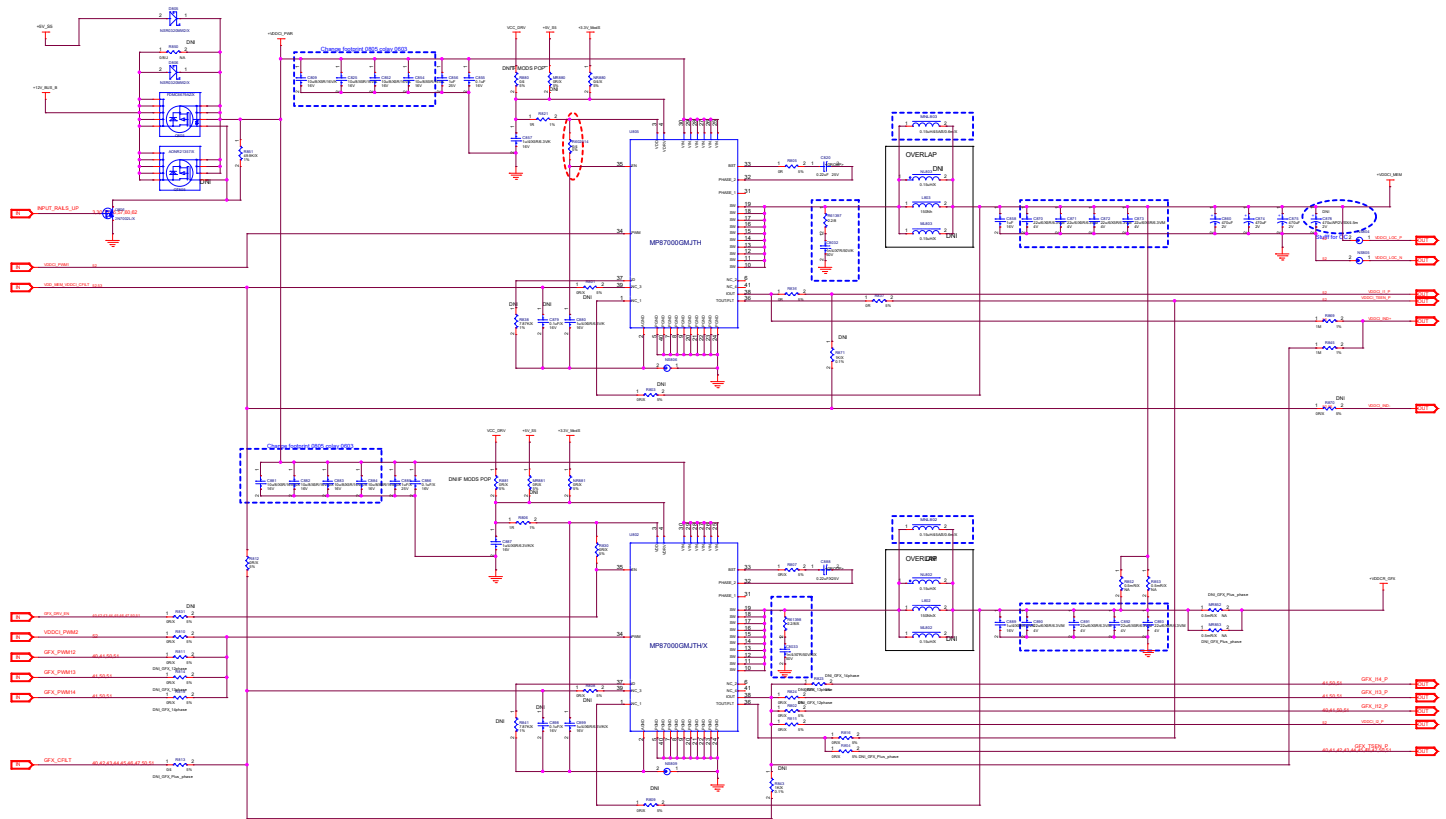
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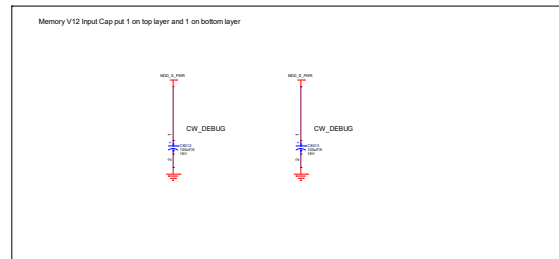
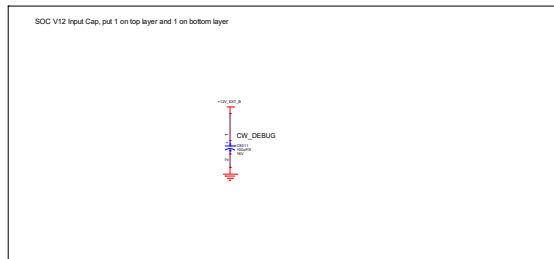
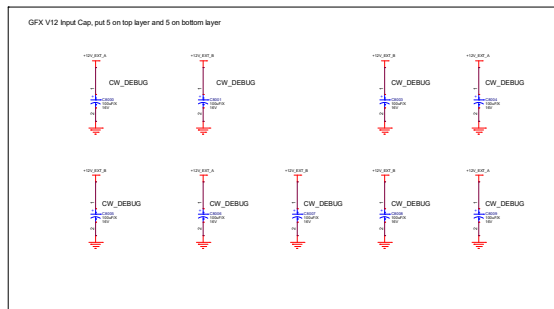
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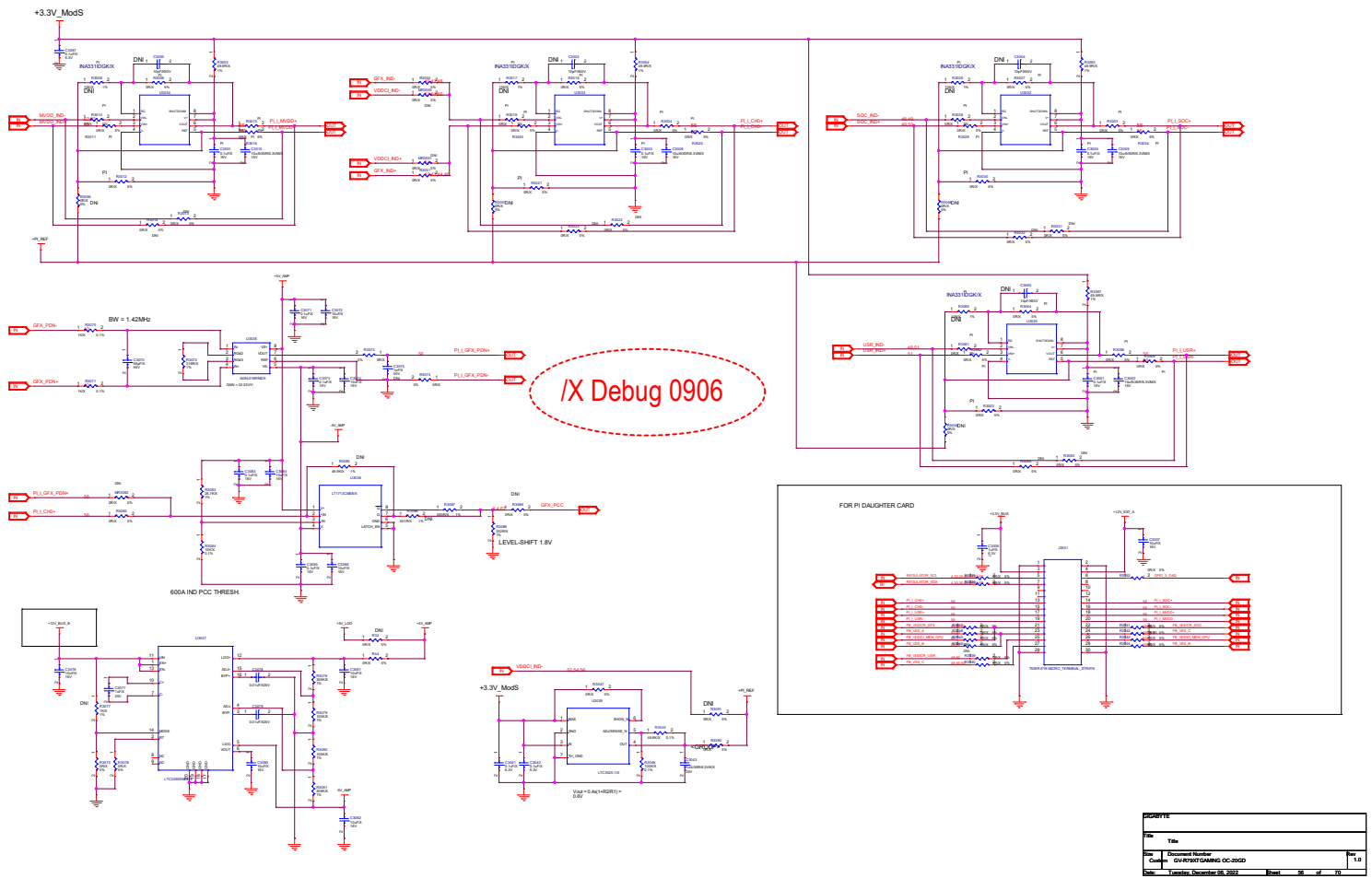


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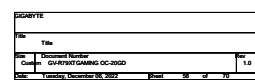
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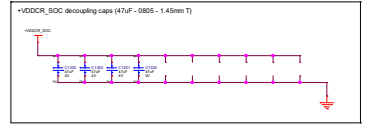
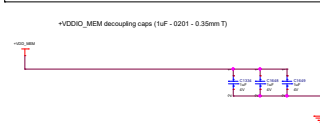
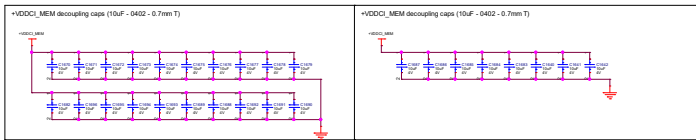
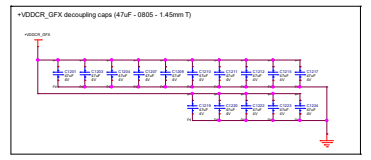
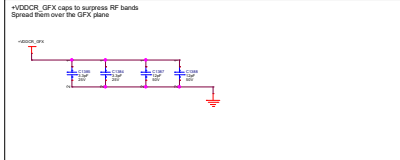
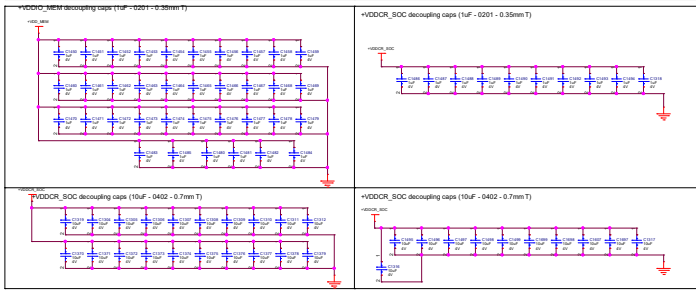
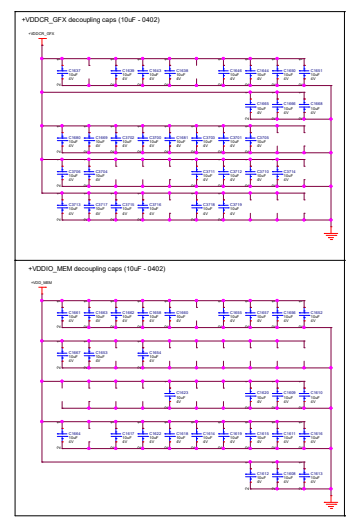
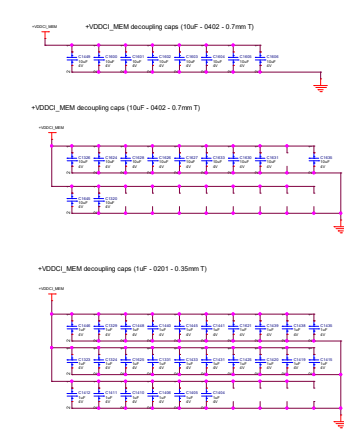
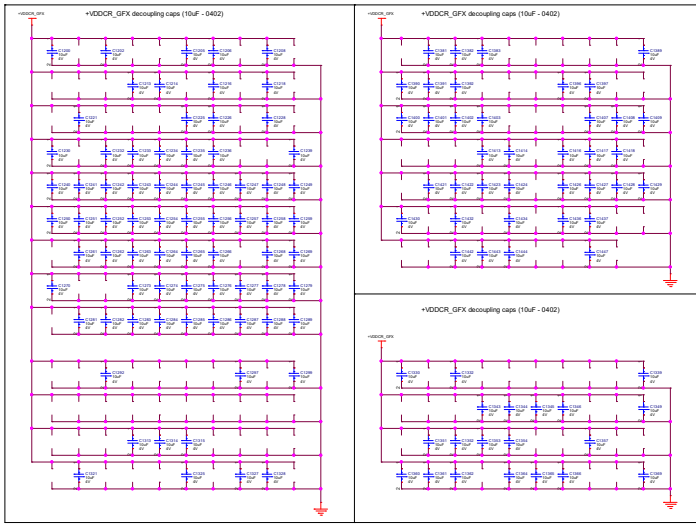


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Date	Tuesday, December 09, 2022	Sheet 20 of 70



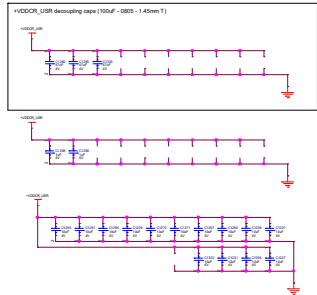
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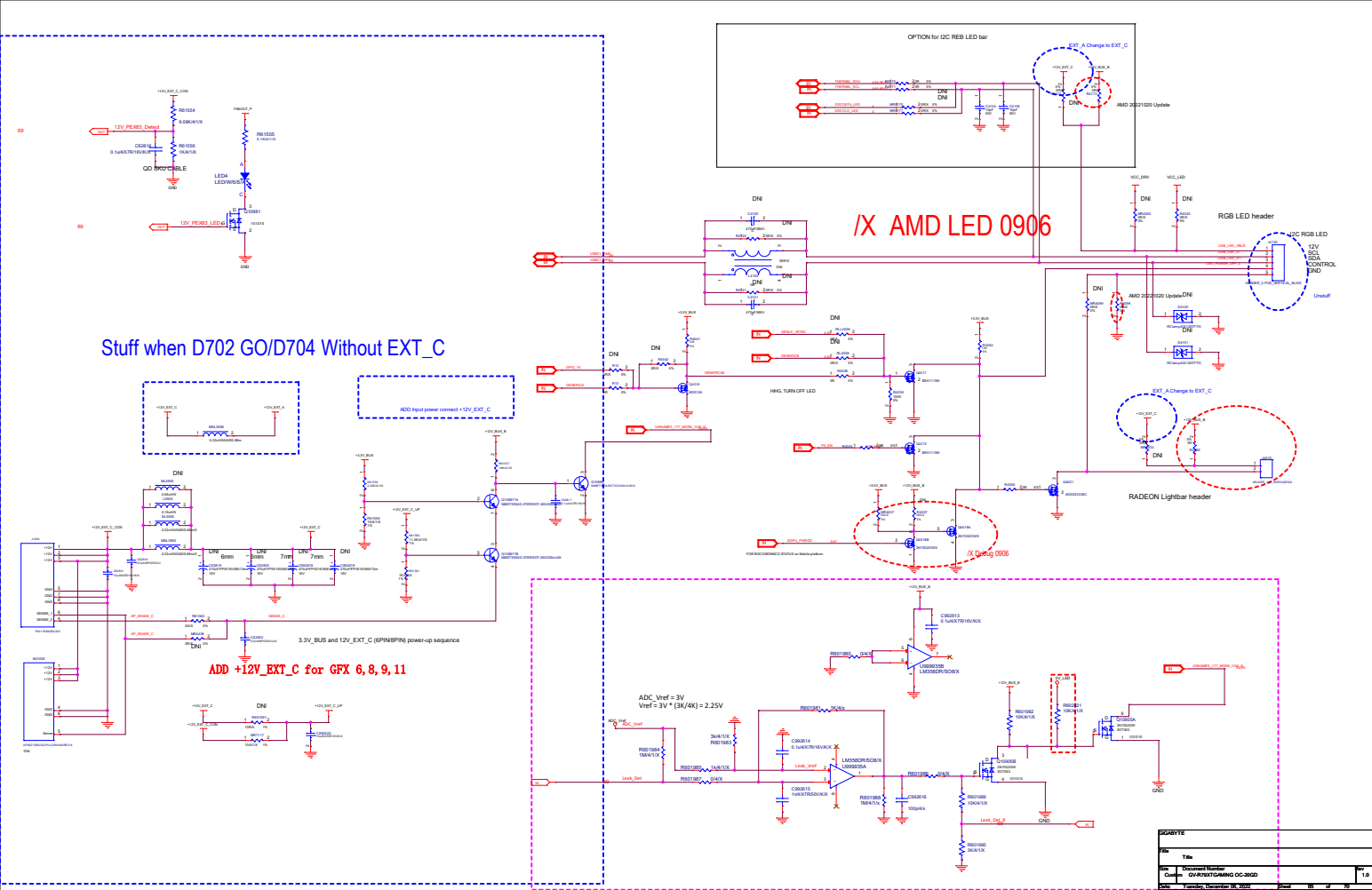
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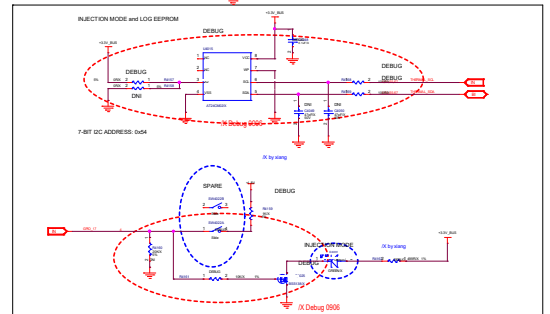
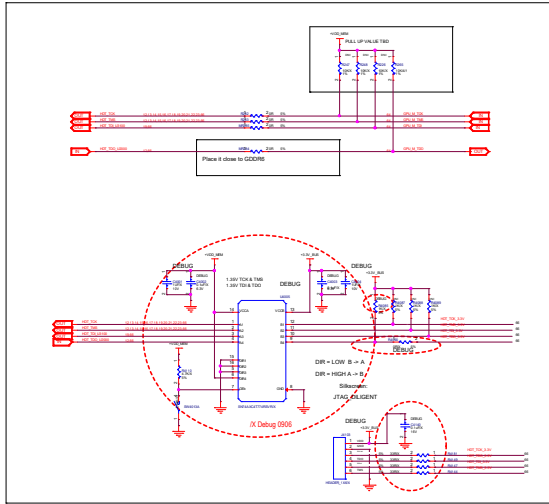
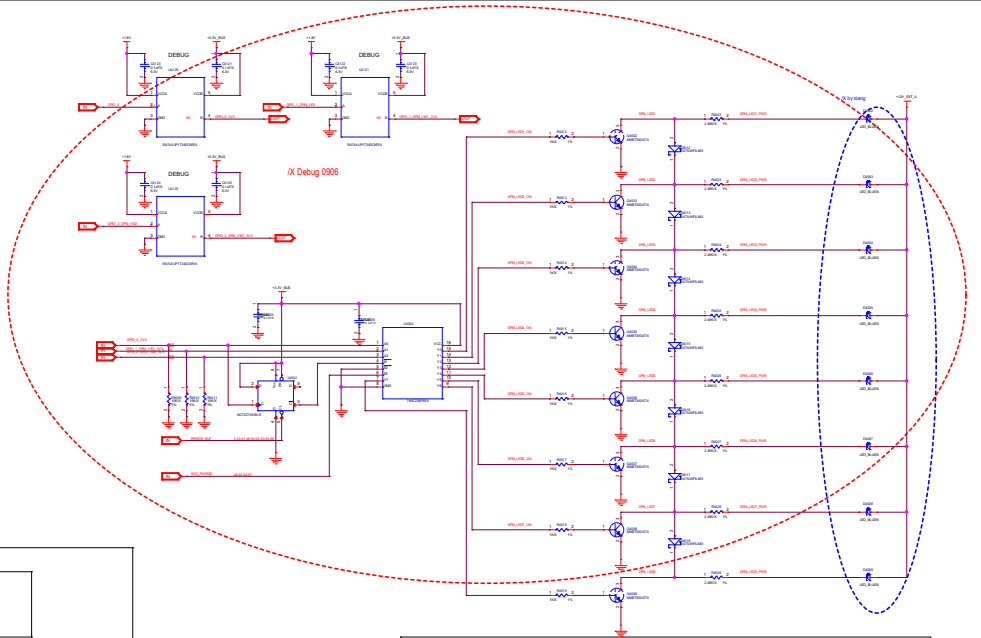






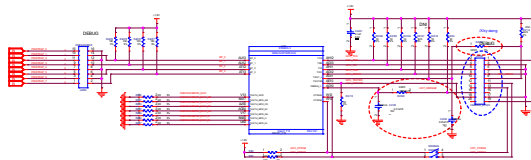
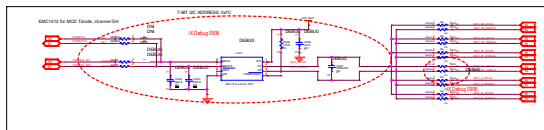
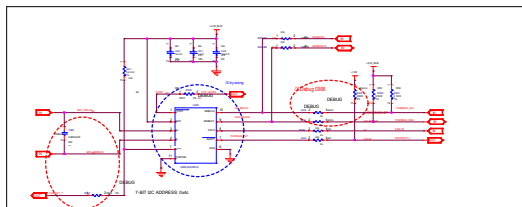
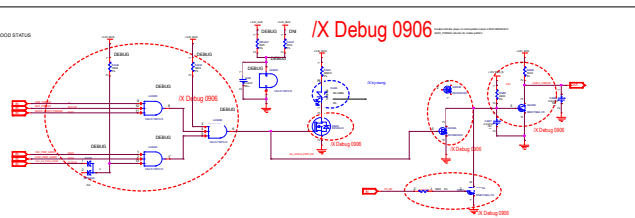
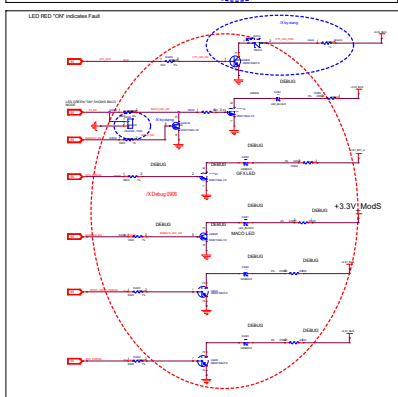
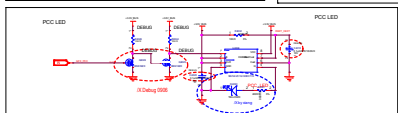
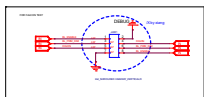
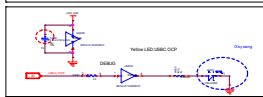
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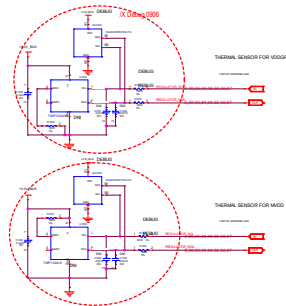
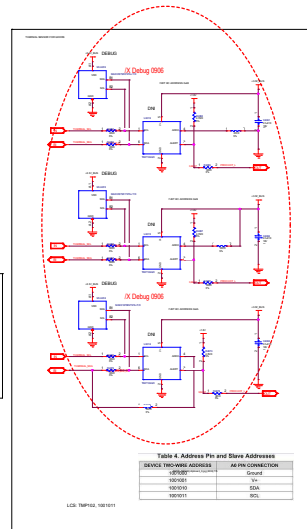


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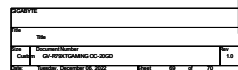


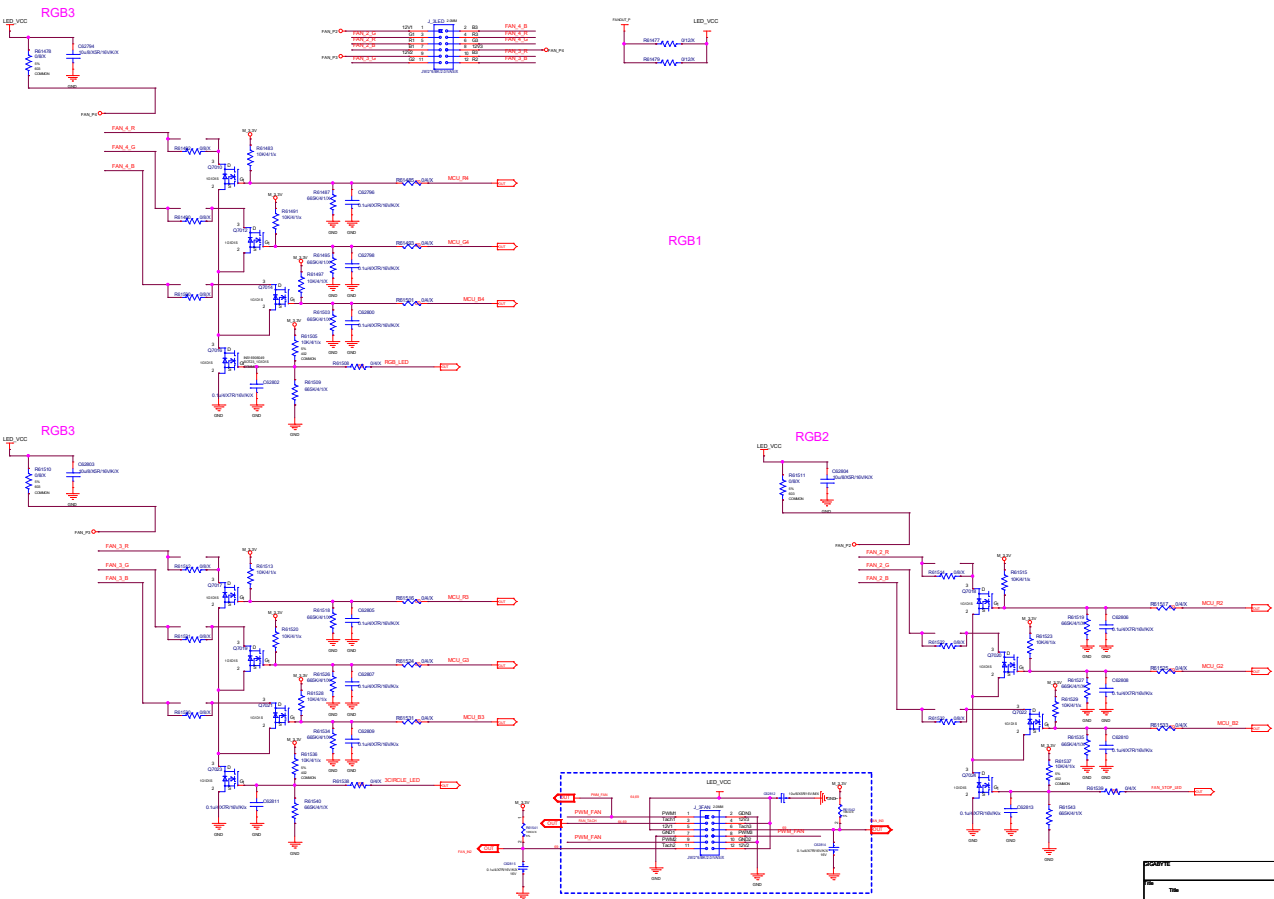
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BP_I2C_TMS	Input - IO **	I/O Pad - 50k Ohm Internal PU	Board Term: 24 Ohm Pullup
BP_I2C_TST_L	Input - IO **	I/O Pad - 50k Ohm Internal PU	Board Term: 24 Ohm Pullup
BP_I2C_TST	Input - GPIO **	I/O Pad - 50k Ohm Internal PU	Board Term: 24 Ohm Pullup
BP_I2C_TSD	Output - GPIO **	Not specified	None: Not Specified
BP_I2C_ADDR_L	Input - GPIO **	I/O Pad - 50k Ohm Internal PU	Board Term: 24 Ohm Pullup
BP_I2C_ADDR_H	Bi-Directional IO	I/O Pad - Open Drain, 50k Int PU	Board Term: 2.2k Ohm Pullup
BP_I2C_ADDR_L	Bi-Directional IO	I/O Pad - Open Drain, 50k Int PU	Board Term: 2.2k Ohm Pullup



Device	Pin	Board Term
SW1	SW1	SW1
THERM	THERM	THERM
PCC	PCC	PCC
LED_RED_V	LED_RED_V	LED_RED_V
PGOOD	PGOOD	PGOOD
I2C_ADDR	I2C_ADDR	I2C_ADDR
THERM_VDDCP	THERM_VDDCP	THERM_VDDCP
THERM_VDD	THERM_VDD	THERM_VDD

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REVISION	
Rev	1.0
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CHECKED BY	
APPROVED BY	
DATE	

